

Integration of a Phase Change Material for Junction-Level Cooling in GaN Devices

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Abstract

Next generation gallium nitride (GaN) RF power transistors offer higher power, higher efficiency and wider bandwidth than competing Si technologies. However, the high power densities available in GaN power transistors create new challenges for heat dissipation. This paper presents a novel micro-scale thermal storage design that involves phase change material (PCM) filled grooves etched in the substrate to remove the heat generated in the active regions of a pulsed-mode GaN transistor. High electron mobility transistors (HEMTs) were fabricated on a GaN-on-Si wafer. Backside patterning and etching were done to thin the Si substrate under the active channel region of the selected transistors. A phase change material (PCM) with a melting temperature of 118°C was deposited in the etched grooves. Electrical measurements were carried out to compare the performance of transistors with and without PCM filled grooves. It was found that the groove etching did not degrade the transistor performance under low power conditions where the junction level heating is not enough to start the PCM melting process. From the current-voltage characteristics at different temperatures ranging from 25°C to 120°C, it was found that at higher temperatures, the current density in the PCM-enabled device was larger than in the reference device, due to the enhanced thermal management. The role of PCM was confirmed when measurements at temperatures well above the melting temperature of the PCM did not show signs of increase in the current density. The maximum current density in the device with PCM material was found to be much more stable under pulsed conditions than in current state-of-the-art devices.

Keywords

Gallium Nitride, Phase Change Material, Junction Level Cooling

Nomenclature

V_g -Gate voltage (V)

V_{ds} -Drain to source voltage (V)

I_{ds} -Drain current at a given drain to source voltage (A)

$I_{ds,max}$ -Maximum drain current (A)

Introduction

The need for high power, high frequency transistors is increasing as RF and microwave applications are becoming more important driven by the tremendous demand for wireless telecommunications. AlGaIn/GaN High Electron Mobility

Transistors (HEMTs) have become the preferred option for solid state amplifiers in the 1-40 GHz frequency range. With an output power density of more than 40 W/mm (output power normalized by gate width) at 4 GHz [1], these devices offer higher power density, higher efficiency levels, lower cooling requirements, and better impedance matching than silicon-based electronics [2]. For a given operating frequency, GaN transistors can run at higher voltages (bias voltages of, for example, 48 V or 65 V in X-band devices) and hence higher output power. Another important application of GaN transistors is high voltage switches in the next generation of power electronics.

In spite of the excellent performance demonstrated by GaN transistors, the extremely high power densities available in GaN devices create new challenges for heat dissipation. The device junction temperature needs to be maintained below 150-175°C to minimize degradation in the transport properties of the semiconductor. Even when operating at the relatively low power densities of 4 W/mm, these devices need to be attached to large heat sinks, which significantly reduce the system scalability.

On a GaN chip, the heat is generated at discrete locations due to the electrical resistance faced by the current as it flows from the source to the drain. In addition, many GaN power amplifiers operate under pulsed mode, i.e., an “ON” or active period followed by an “OFF” or inactive period, which induces rapid changes in channel temperature during each cycle. In this paper we propose a new cooling technology based on a phase changing material (PCM) which enables heat dissipation, operation at much higher power densities and the use of silicon substrates instead of the much more expensive silicon carbide (SiC) substrates typically used in GaN electronics to improve heat dissipation. This approach is based on the increase of the effective heat capacitance of the material layers (via thermal storage material such as PCM) nearest to the transistor junction to reduce the peak temperature and the transient changes.

Concept

The new cooling approach presented in this paper takes advantage of the heat of fusion in PCMs to increase the heat capacitance of the transistor structures at the junction level. The melting point of the PCM creates a “stop” for the peak junction temperature provided there is sufficient PCM material to absorb all of the heat generated during the “on” pulse and relatively long inactive time to release the heat and

refreeze all of the PCM. An optimal amount of PCM will prevent the chip junction temperature from rising and falling rapidly, making the chip isothermal over the entire duty cycle, which is ideal in terms of increased device reliability. In the proposed chip level cooling application, the transients are fast, so only a small amount of PCM (less than a microgram) is required for this application, which makes the integration of PCM into the device level very feasible.

GaN-based transistors were fabricated on the front side of a GaN-on-silicon wafer and several grooves were etched in the back-side of the silicon substrate using standard microfabrication technology. The groove-type design extends the surface area for heat transfer between the PCM and groove walls and improves the accessibility to hot spots. These grooves were filled with an appropriate amount of PCM, after which the electrical performance of the GaN devices was tested. Figure 1 shows a summary of the mask layout used during the device fabrication. A row of transistors with back Si-etch was followed by a row of transistors without back Si-etch. This design allowed the devices with grooves and without grooves to be tested under the same conditions.

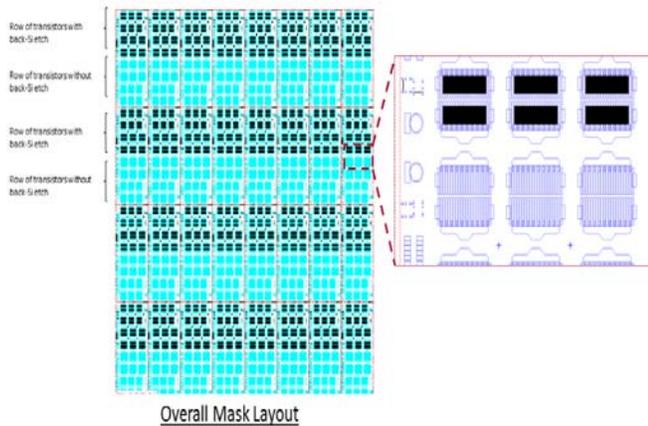


Figure 1: Top View of Mask Layout for fabricated GaN transistors with integrated PCM cooling.

Fabrication

Prototype devices were fabricated to experimentally test the concept of junction level thermal storage in devices operated under pulsed conditions. The epitaxial structure of the wafer consisted of a 25 nm AlGaN barrier layer on a 1.8 μm GaN buffer layer grown by metal organic chemical vapor deposition (MOCVD) on a 550 μm Si substrate with (111) orientation. The process flow of the device fabrication is shown in Figure 2. It starts with the patterning and isolation of individual transistors. The device isolation was performed through mesa etching with a Cl_2 -based Reactive Ion Etching plasma system. Then, the source and drain ohmic contacts were defined and deposited through electron beam deposition. A Ti/Al/Ni/Au metal stack was used and annealed at 870 $^\circ\text{C}$ for 30s to form the ohmic contacts. A Ni/Au/Ni gate electrode was then defined by optical lithography and deposited by electron beam deposition. The devices were passivated with a 25 nm Al_2O_3 dielectric deposited by atomic

layer deposition, and openings were etched in the dielectric using buffered oxide etch.

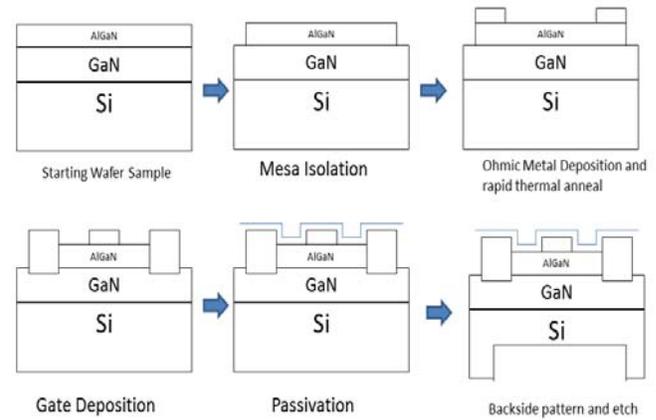
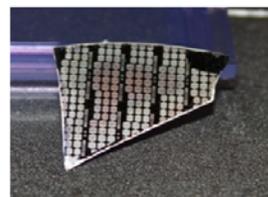
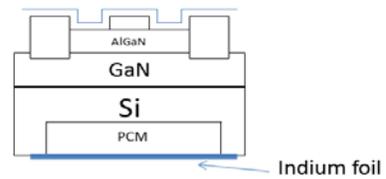


Figure 2: Process flow for the GaN HEMT

Then, the PCM thermal storage structure was fabricated by first patterning the region where the PCM material would be deposited. The silicon substrate was etched through a Bosch dry etch process, and the photoresist was removed by standard cleaning with solvents. The device fabrication was finished with the deposition of the PCM into the silicon grooves by melting the PCM material in the grooves. Adequate care was taken to remove the excess PCM lying on the chip outside the groove. The PCM was then encapsulated with a thin indium foil. Figure 3 shows the cross-section of a fully fabricated device, as well as a top-view and a bottom-view image of the fabricated chip.



Sample Front side



Sample Back side

Figure 3: Fabricated GaN sample--(Top) Cross-sectional image of fully fabricated AlGaN/GaN HEMT with an integrated PCM cooling system, (bottom-left) Top-view image of a fabricated chip, (bottom-right) Bottom-view image of the fabricated chip showing the indium foil encapsulation

Breakdown Voltage Measurements

The first test on these fabricated devices was to confirm that under low power conditions the groove fabrication process does not degrade the transistor performance. Under these conditions, the PCM does not play a role as the junction

level temperature does not rise above the melting temperature of PCM. The 3-terminal off-state breakdown voltages of devices with PCM and devices without grooves were measured. To keep the device in the “off-state”, the gate voltage was kept constant at $V_g = -8$ V and the drain-to-source voltage was swept up until the drain current reached 1mA/mm. The values of breakdown voltage, V_{bk} , for the two cases, devices with PCM filled grooves (127.5 V) and devices without grooves (122.2 V) were similar, as shown in Figure 4.

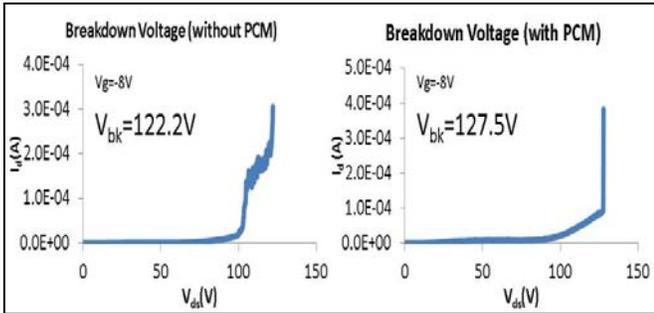


Figure 4: Three-terminal off-state breakdown voltage of GaN transistors with and without PCM

DC V_{ds} - I_{ds} Measurements at Different Chuck Temperatures

Negative differential resistance in the saturation region of the V_{ds} - I_{ds} curve of GaN transistors is an indication of self-heating [3]. The magnitude of the decrease of drain current in the saturation region correlates to the magnitude of device self-heating. Figure 5 shows the current-voltage (I - V) characteristics of devices with PCM-filled grooves (blue empty circles) compared to control devices without grooves (red lines). At room temperature, the normalized values of drain current ($I_{ds}/I_{ds,max}$, the value of the drain current at a given drain-to-source voltage divided by the maximum drain current) for the PCM filled devices are similar to the devices without grooves. With increasing chuck temperature (100°C and 120°C), the difference between the red and blue lines increases. This indicates that the difference in the decrease of relative drain current between PCM and non-PCM devices is larger at higher temperatures. The increase in drain voltages results in increased self-heating and higher junction temperature. The current density in the PCM-enabled devices is higher than the value in the reference devices; this difference is associated with the enhanced thermal management of the PCM device and the subsequent reduction in self-heating. The role of PCM is confirmed when the chuck temperature is increased to 140°C which is well above the melting temperature of PCM. Under these conditions, the V_{ds} - I_{ds} curve characteristics are similar to those at room temperature, because the melted PCM no longer acts as a thermal storage.

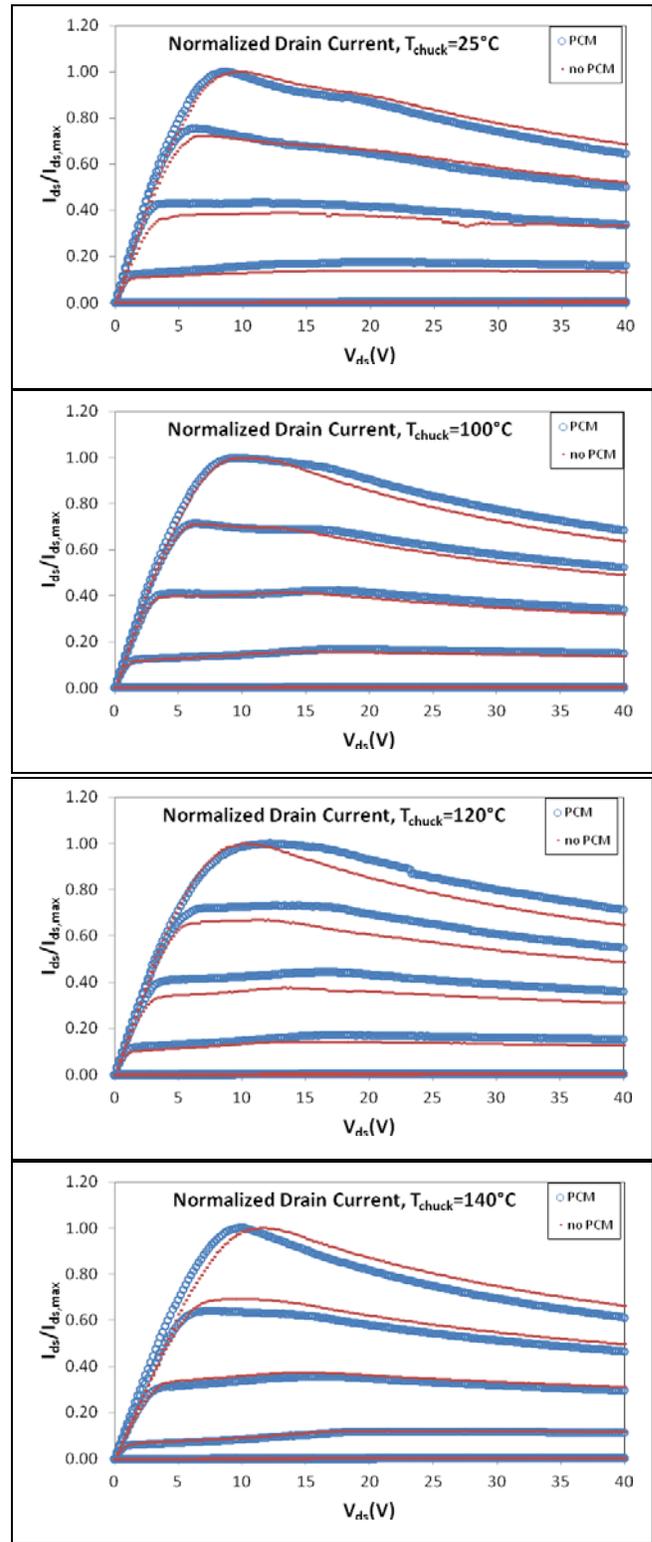


Figure 5: Normalized values of drain current ($I_{ds}/I_{ds,max}$, the value of the drain current at a given drain-to-source voltage divided by the maximum drain current) to illustrate the self-heating effect.

Pulsed IV Measurements

Pulsed current-voltage (I - V) measurements were performed on the devices with PCM-filled grooves and

devices without grooves. The chuck temperature was set to 95°C to be able to operate the small devices that were fabricated in this project under thermal conditions similar to what scaled devices encounter. At each pulse width, the PCM filled groove measurement was followed by the measurements on devices without grooves, before going to the next pulse width. This procedure allowed for enough time (in the range of minutes) for the re-solidification of the melted PCM. Each data point in Figure 6 represents the maximum drain current at the respective pulse width divided by the overall maximum drain current for a single pulse. As the pulse width decreases, the maximum current through the device increases due to reduced device self-heating. As evident from Figure 6, the maximum current density in the device with PCM material is more stable with the pulse width than in the standard device. The device performance in terms of current density shows 10% improvement due to enhanced thermal management. This improved performance demonstrates the role of PCM as a thermal storage to reduce the temperature increase in the device. It is expected that the performance improvement will be substantially higher after further optimization in terms of groove size and location. A computational model is being developed to perform this optimization.

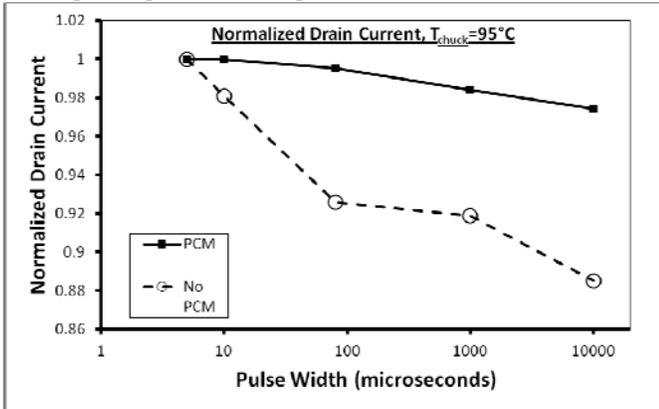


Figure 6: Maximum drain current at the respective pulse width divided by the overall maximum drain current from pulsed IV measurements for devices with and without PCM.

Conclusions

This paper presents a novel micro-scale thermal storage design to remove heat generated in the active regions of a pulsed mode gallium nitride transistor. High electron mobility transistors were fabricated on GaN grown on a Si substrate. Backside patterning and etching were done to thin the Si substrate under the active channel region of selected transistors and a PCM was deposited in the etched grooves. The groove etching did not degrade the transistor performance under low power conditions where the junction level heating is not enough to start the PCM melting process. From the DC current-voltage characteristics at different temperatures, it was seen that the difference in the decrease of relative drain current between PCM and non-PCM devices is larger at higher temperatures (as much as a 7% difference). The role of PCM was confirmed when measurements at temperatures well above the melting temperature of PCM did not show signs of increase in the current density. The maximum current density in the device with PCM material was found to be much more

stable under pulsed conditions than in current state-of-the-art devices.

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