The Affect of Device Level Modeling on System-Level Thermal Predictions

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ABSTRACT

Thermal management is important for the performance and reliability of today's high power and high density electronics systems. The thermal architecture between the device and heat sink can quickly become very complex when designing for ideal operating temperatures. In order to predict the temperature rise, it is desirable to have a simple modeling technique which reduces the amount of time and effort required to obtain accurate results. Often, the heat flux of the device is based on either the die area or the case area. Complication occurs when simplifying the contact area of a given component.

Detailed analyses have been performed for two different cases that show the importance of die-level modeling. In the first case, models of an insulated gate bipolar transistor (IGBT) attached to a cold plate are compared to determine the cold plate temperatures when assuming uniform heat flux, and when modeling from the device level. The different analyses results in a heat sink ΔT that differs by 33%. In the second case, a heat spreader is used to cool several high power components. The heat generation areas of the components are significantly smaller than the case footprint. A detailed look at the device level spreading reveals a difference in maximum temperature of 14.5°C between the results of the different modeling techniques used.

KEY WORDS: thermal modeling, electronics cooling, power electronics, heat spreading

NOMENCLATURE

Greek symbols

ΔT	Temperature difference (°C)
k	Thermal conductivity (W/m-K)

Subscripts

j-c	Junction to case
c-s	Case to sink
j	Junction

INTRODUCTION

Background

As the next generation of electronic devices find their way into industry use, their successful implementation will depend on thermal management. Heat dissipation is the limiting factor on the power levels of modern electronics [1]. The dependency between expected catastrophic failure rates and junction temperature is well known [2]. Heat dissipation is currently a limiting factor, and will continue to be so as electronics approach heat fluxes as high as $1000 W/cm^2$ [1].

Since thermal design can determine the success of an electronics system, it is vital to determine feasibility prior to production. Therefore, simulating thermal performance has become routine in most design processes [3]. Finite element analysis (FEA) and/or computational fluid dynamics (CFD) are numerical approaches used to model solid and fluid systems. Thermal modeling allows electronics to be examined in multiple environments and operating conditions at a significantly reduced cost compared to physical prototyping and testing. It is critical, however, that the model accurately represents the physical device.

Accurate modeling of heat generation requires the designer to understand the thermal stack-up of the particular device. This information is provided by the device manufacturer and is a fixed thermal resistance in the overall system. In many instances the component heat flux is assumed to be uniform across the device footprint since the long lead times associated with detailed analysis are often not practical [4]. This assumption may not be accurate depending on the heat spreading within the device.

Thermal models of two different cases are presented in this paper. The first case reviews an approach used to model an IGBT (Insulated Gate Bipolar Transistor) mounted to a liquid cooled cold plate. The second model examines smaller chips mounted onto a heat sink. In both cases the thermal solution is first studied assuming uniform heat flux generated off the foot print of the electronic device, followed by a die level analysis. The detailed models show that the uniform flux assumption may or may not be conservative. In either case, the uniform flux assumption represents a source of error in the model.

Heat Generation and Spreading in Electronics

On a chip, heat is generated at discrete locations due to the electrical resistance faced by current as it traverses from source to drain circuitry, with the heat generation slightly favoring the drain side. Figure 1 depicts heat generation within a typical semiconductor [5]. The heat flux generated from these individual transistors must then conduct through multiple layers of various metals, interface materials, etc. in what is commonly known as the thermal stack-up. Each layer adds to the overall thermal resistance of the device, resulting in increased peak junction temperatures.

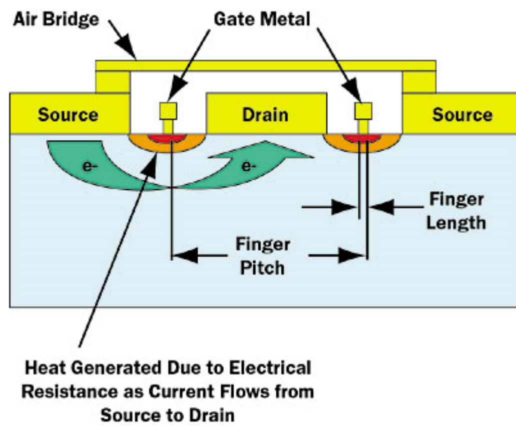

Figure 1: Schematic detailing heat generation within a chip [5]

In a typical stack-up, the heat conduction path from the chip to the heat sink is as follows: chip → solder → tab → epoxy → metal baseplate → thermal interface material (TIM) → PCB → TIM → heat sink [5].

Power Electronics
One specific example of power devices is the Insulated Gate Bi-polar Transistor (IGBT), which is a relatively large semiconductor device and is prone to large thermal gradients.

In the conventional assembly, the IGBT dies are first mounted onto a layer of direct bond copper (DBC) because it provides excellent electrical and thermal properties and closely matches the coefficient of thermal expansion (CTE) of the power devices. The DBC layer is attached to a layer of aluminum silicon carbide (AlSiC), which provides additional heat spreading and acts as a CTE transition layer between the DBC and heat sink. Thermal interface materials (TIM) are used to join the IGBT and the heat sink. Typical heat generation for IGBTs is on the order of kilowatts, so liquid cooled heat sinks are often required to manage the large amount of heat.

The interface between separate components may be a significant thermal resistance. Due to surface roughness there exist finite contact resistances with interspersed gaps, often filled with air. Heat transfer is therefore governed by conduction across the points in contact and radiation across the gaps [8]. Thermal interface materials (TIMs) are used to fill the voids between interfaces thereby reducing the thermal resistance. Typical TIMs consist of thermally conductive polymers and greases, graphite pastes and sheets, and phase change materials. A thermal resistance value is usually provided by the manufacturer of the TIM and is often a function of contact pressure.

Microelectronic Systems
On the product data sheet, the thermal resistances of microelectronic systems is similar to that of power electronics, however the internal structure differs greatly. For micro-electronic systems, the junction to case resistance is the result of wafer-metal interconnects, wire bonds, and solder joints between the chip and printed circuit board (PCB). The junction to case resistance may be considered a constant value defined by the manufacturer which cannot be altered [7].

Many designs that fall into the category of micro electronics feature components mounted to a printed circuit board (PCB). PCBs are normally made of FR4 which is a glass-reinforced epoxy laminate. The thermal conductivity of FR4 is relatively poor, however copper embedded within the board (in the form of planes) aids thermal performance. As a result, the in-plane conductivity of a printed circuit board is enhanced. This must be considered when designing heat sinks because the heat flux leaving the circuit board is a function of the spreading within the case. The maximum junction temperatures may be incorrectly represented if this is not taken into account.

Due to computational limitations, simplifications are often required [8]. One approach used to predict temperature gradients assumes uniform heat applied across the case of the device. A more conservative approach would be to use the die/chip area. Both approaches may result in unrealistic ΔTs. It is typical to observe non-uniform heat flux profiles on the heat sink due to the high power densities applied to separate dies within the overall package. This mal-distribution of heat must be accounted for to obtain accurate thermal gradients. Conversely, using the die footprint to predict ΔT results in over predicting thermal gradients since some heat spreading within the package is observed. Device level modeling is required to accurately predict the system level ΔT.

POWER ELECTRONIC MODELING

Boundary Conditions
In this study a thermal model of an IGBT mounted to a liquid cooled cold plate is analyzed to determine the maximum junction temperature. Cold plate modeling begins with assuming uniform heat flux is applied to the footprint of the components. The IGBTs however have separate heat generating die within the case, which generate a non-uniform heat flux profile. A device level analysis was also conducted on the IGBT module. The stack-up for a typical IGBT module is shown in Figure 2.

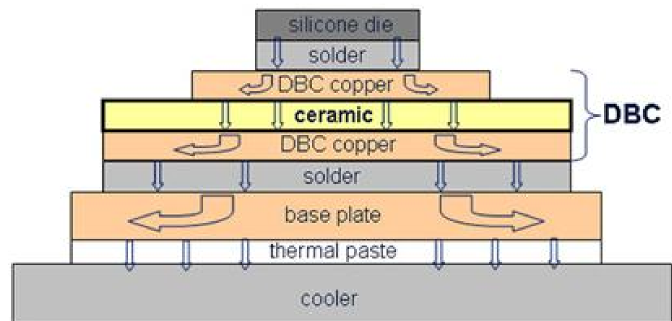

Figure 2: Thermal Stack Up for a Typical IGBT [9]

The analysis was conducted for a total heat load of 4090W. An initial model was run that used a uniform heat flux applied to the base of the IGBT. The next model had the heat load divided between the dies within the IGBT. In both models the IGBT is attached to a cold plate. A section of the cold plate was also modeled which represents the tubing layout beneath the IGBTs in the full system. The flow boundary condition assumed uniform fluid flow applied equally to the tubes with an inlet temperature of 43°C. The boundary conditions for this model are shown in Figure 3.

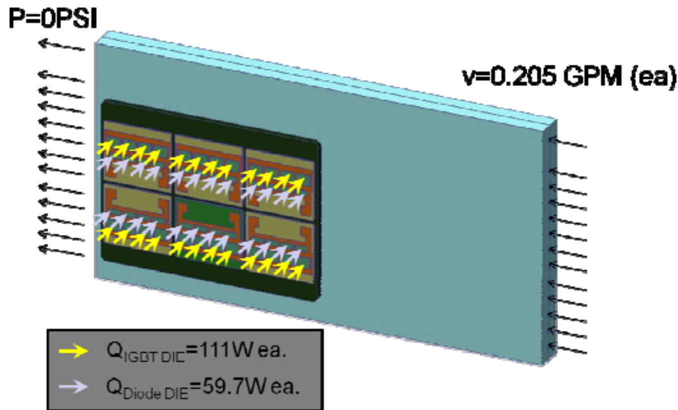

Figure 3: IGBT Device level boundary conditions

Results

The preliminary model that assumes a uniform heat flux off the IGBT case predicted a maximum cold plate temperature of 74°C. Subtracting the max cold plate temperature from the inlet water temperature results in a 31°C cold plate ΔT. Adding the calculated $\Delta T_{j\text{-}c}$=25°C and $\Delta T_{c\text{-}s}$=2°C based thermal resistances defined by the manufacturer; the predicted junction temperature is 101°C. This is well below the maximum junction operating temperature of 120°C.

The results of the device-level analysis are displayed in Figure 4, which predict a maximum junction temperature of 112°C. As the figure shows, there are localized hot spots below the heat generating components, as expected. The increased heat flux below the dies raised $\Delta T_{c\text{-}s}$ to 4°C as well as the maximum cold plate temperature to 83°C. This corresponds to a cold plate ΔT=40°C, which is 9°C higher than when modeled with a uniform heat flux. When including the change in interface ΔT, the junction temperature increases at total of 11°C.

An image of the heat flux off the case of the IGBT is shown in Figure 5 along with a plot showing the heat flux ratio. The heat flux ratio is determined by dividing the local heat flux by the uniform heat flux. This plot shows there is nearly 2X the heat flux off the case below the die compared to the rest of the IGBT.

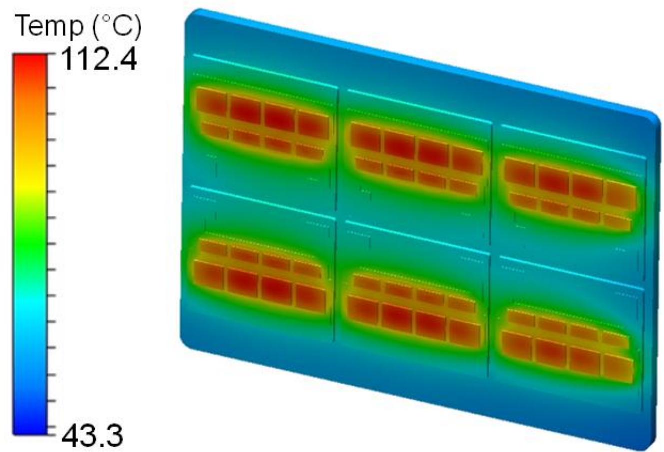

Figure 4: Device level model results

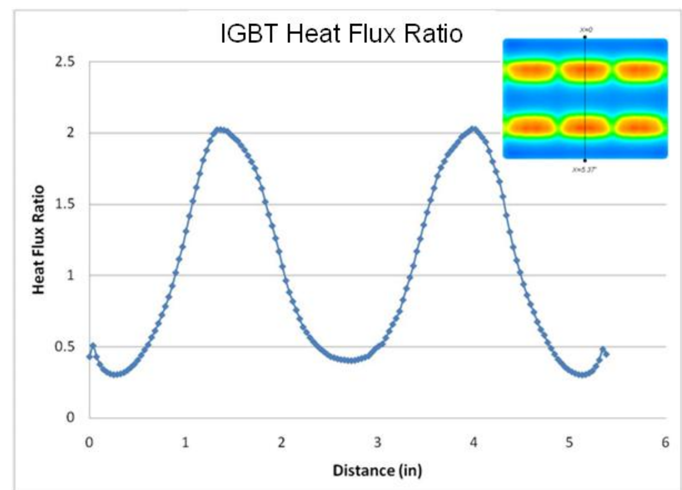

Figure 5: Heat Flux Profile on the IGBT Case (at cold plate surface)

MICRO ELECTRONICS MODELING

In this analysis, a heat spreader was designed to manage the heat loading from six separate power sources. The edges of the heat spreader are held into a cooling channel by clamps, so the primary route for heat dissipation is by conduction to the edge of the spreader where it is transferred to the liquid coolant, which maintains a cooled edge temperature of 71°C. Two of the six heat sources cover a major area of 27mm x 27mm each and generate 4W and 2W, respectively. These components are located near the center of the heat spreader, the greatest distance from the cooled surface. Because they are relatively low power components, they are not sensitive to thermal limits in this application. The majority of the heat load is generated by the remaining four components, which each produce 25W in a 33mm square footprint. These components have been strategically placed near to the cooled surfaces to minimize the length of conduction between the component and the cooled surface. Further details provided by the component manufacturer reveal that the actual heat

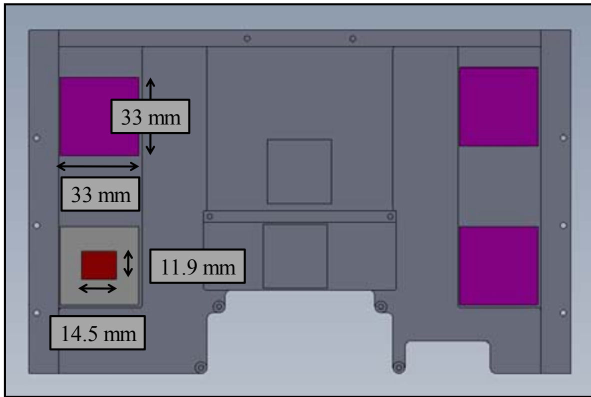

Figure 6: Micro electronics layout showing the component footprint and the actual heat generation area mounted on a heat spreader

generation ("high heat") area of the component is a concentrated region which measures 11.9mm x 14.5mm. Figure 6 shows the location of the four high power components and the dimensions of their footprint as well as the heat generation areas.

The four high powered components have a maximum allowable junction temperature of 85°C. This permits a rise of 14° over the cooled edge temperature of 71°C.

Boundary Conditions

First, a baseline model (Analysis 1) was developed with each of the components mounted to a pure aluminum spreader plate. The spreader plate was modeled as 6061 T6 aluminum with a thermal conductivity of 167W/m-K. The heat loading from the 6 electronic components are simulated as surfaces in direct contact with the aluminum spreader, totaling the 106W described in the previous section. The results of the baseline analysis show that the allowable temperature limits were surpassed by more than 15°C, indicating the need for a higher performance heat spreader to be used between the components and the liquid cooling regions. In order to improve the effective conductivity of the spreader plate, heat pipes were embedded in the plate to aid in transporting heat from each component to the cooled edges.

Three heat pipes were embedded beneath each of the high power components. 4mm (.157") diameter heat pipes of varying length were used to transport heat from the high flux regions to the cooled surface. Although the external physical geometry of the plate was not changed by adding the heat pipes, the thermal conductivity was improved significantly.

A second analysis (Analysis 2) was performed using the same boundary conditions and heat input areas as Analysis 1, only with the addition of heat pipes. The majority of the spreader plate is still aluminum 6061, but the areas that now contain heat pipes have been assigned significantly higher conductivities to represent the improvement resulting from the two phase heat transfer. A constant temperature boundary condition of 71°C was assigned to the areas representing where the spreader plate meets the cooled edge.

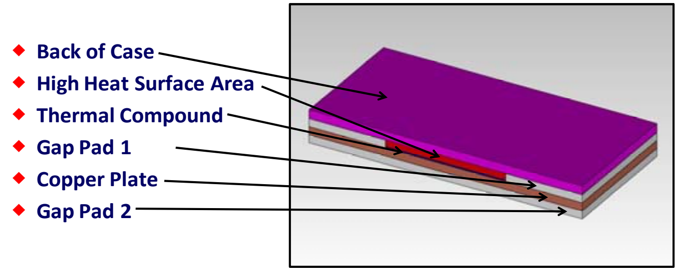

Figure 7: Cross sectional view showing micro electronics component stack up from Analysis 3

To use the full 33mm x 33mm footprint of the component would incorrectly represent the heat flux into the spreader plate. However, to model the exact heat generation area of 11.9mm x 14.5mm does not account for heat spreading within the component stack up itself, which is an equally inaccurate boundary condition for a thermal model. Rather, a technique must be used that addresses spreading within the case while still conservatively estimating the heat flux into the heat spreader.

A higher than acceptable junction temperature of Analysis 2 prompted a second look at the construction of the component and how it is mated to the heat spreader. A new device level model (Analysis 3) was proposed which more accurately represents the inner workings of the case. This model, shown in Figure 7, includes a copper spreader plate (1.0mm thick, 391.0W/m-K), thermal gap pads (0.8mm thick, 14.0W/m-K) and thermal compound (0.18mm thick, 7.5W/m-K), all of which contribute to an altered thermal structure that is not captured in Analysis 2. This model also accounts for the high heat surface area which was represented as a volume (0.82mm thick, 80.7W/m-K) as well as the back of the case (1.1mm thick, 4.0W/m-K). The boundary conditions were kept constant although the heat load is now directly input to the surface of the "High Heat Surface Area" that faces opposite the aluminum spreader instead of being assigned to the heat spreader itself.

Results

A thermal image of the results from Analysis 2 is shown in Figure 8 (left side). The intensity of the higher flux components is evident when compared to the results of Analysis 3 (right side of Figure 8). The local temperature gradient between the Analysis 2 component hot spot and the heat spreader is roughly two times that of Analysis 3. This aligns with the reduction in heat flux between the two cases. The heat spreading in the component stack up increases the effective footprint which lowers the flux into the spreader. The Analysis 2 maximum component temperature is 98.4°C which surpasses the allowable maximum temperature of 85°C significantly. By more accurately modeling the internals of the component package in Analysis 3, the maximum junction temperature was reduced to 83.9° which is safely within the 85°C allowable temperature constraint.

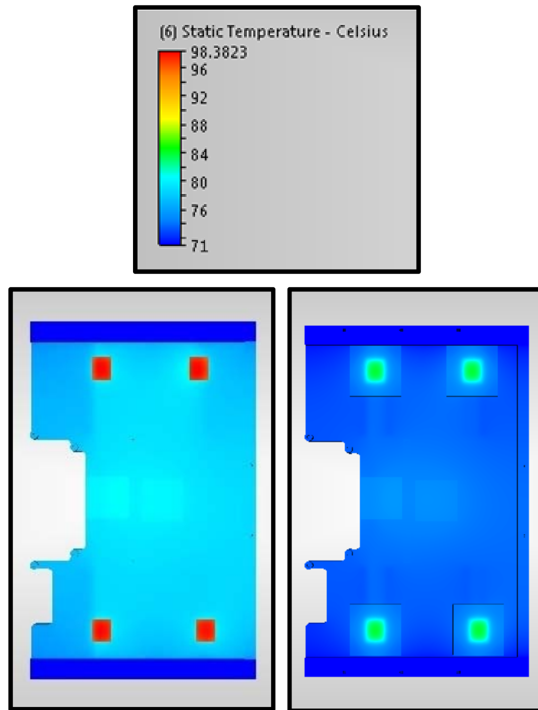

Figure 8: Thermal image of the uniform flux model on the left (Analysis 2) and the die-level model on the right (Analysis 3)

CONCLUSION

Two examples which prove the importance of device level modeling have been reported. In the first, a detailed IGBT model was developed to determine the change in flux distribution caused by the internal construction of the device. The results are relevant because the temperature difference realized by the detailed model is significant, demonstrating a temperature increase of 11°C. In this analysis applying a uniform heat flux to the heat sink under predicts system ΔT. This temperature change correlates to 33% difference in combined interface-heatsink ΔT.

The second supporting example features a much smaller, lower power condition with a similar result. By breaking the device down into the individual case components, the thermal stack-up was more accurately represented. The different modeling approaches affect the maximum temperature by 14.5°C. Here applying the heat flux of the die foot print to the heat sink over predicts system ΔT.

From an engineering perspective, this concept is important. Often times, discrepancies at the device level affect decision making with regards to system performance or heat sink design and layout. It is critical that device level modeling be performed accurately to help the higher level system to be designed most efficiently and perform as expected.

As the demand for higher output continues to test the limits of electronic components, the need for accurate thermal solutions will only increase in its level of importance. The designer's ability to accurately predict a system's thermal behavior, starting at the device level, will be paramount to achieving performance goals.

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